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In re Patent Application of: Eugene H. Cloud
Title: HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY
Attorney Docket No.: 303.663US1

PATENT APPLICATION TRANSMITTAL

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X Utility Patent Application under 37 CFR § 1.53(b) comprising:
- X Specification (12 pgs, including claims numbered 1 through 21 and a 1 page Abstract).
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HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY

Technical Field of the Invention

The present invention relates generally to semiconductor memory and in particular to data compression and decompression in a dynamic random access memory device.

Background of the Invention

Semiconductor memory devices such as dynamic random access memory (DRAM) devices are widely used to store data in computers and electronic products. One important criterion in a DRAM device is storage density. As semiconductor technology advances, designers strive to design new generation of DRAM device with a higher storage density.

There are many methods used in designing a DRAM device to achieve a higher density. One method is reducing the size of each of millions of cells in a DRAM device thus increasing the number of cells and consequently increasing the overall storage density of the device. Another method is stacking the cells vertically, this in effect, doubles the storage capacity. There are other methods of designing a DRAM device to achieve high storage density.

There is a need for a method to achieve even higher storage density for a DRAM device using other techniques.

Summary of the Invention

The present invention increases a storage density of a semiconductor memory device. In particular, the invention includes an apparatus and method of compressing and decompressing data in a DRAM device.

In one embodiment of the invention, the memory device includes a main memory, an input/output buffer, a cache memory connected between the main memory

and the input/output buffer, and a compression and decompression engine connected between the main memory and the cache memory.

In another embodiment of the invention, the memory device includes a main memory, a cache memory connected to the main memory, a compression and decompression engine connected to the main memory and the cache memory, and an error detection and correction engine connected to the main memory and the compression and decompression engine.

Yet another embodiment of the invention provides a method of increasing a storage density of a memory device. The method comprises forming a main memory in a semiconductor chip, forming a cache memory, forming a compression and decompression engine in the same chip, and connecting the compression and decompression engine between the main memory and the cache memory.

Brief Description of the Drawings

Figure 1 illustrates a prior art a memory device;

Figure 2 illustrates a memory device of the present invention.

Figure 3 illustrates a memory device of Figure 2 including an error detection and correction (ECC) engine;

Figure 4 illustrates another embodiment of a memory device.

Figure 5 illustrates a computer system incorporating the memory devices of Figures 2-4; and

Figure 6 illustrates an exemplary environment including memory device of the present invention.

Detailed Description of the Invention

The following detailed description of the preferred embodiments refers to the accompanying drawings which form a part hereof, and shows by way of illustration specific preferred embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized

and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the invention is defined only by the appended claims.

Figure 1 illustrates a prior art a memory device 100. Memory device 100 includes a cache memory 102 connected between a main memory 104, and an input/output (I/O) buffer 106. Main memory 104 typically comprises dynamic random access memory (DRAM) devices and comprises one or more memory banks, indicated by BANK 1-N. Each of the memory banks BANK 1-N comprises a plurality of memory cells arranged in rows and columns. Row decode circuit 108 and column decode circuit 110 access the rows and columns in response to an address, provided on address bus (ADDRESS) by an external controller, such as a microprocessor. I/O data buffers 106 connects to data communication lines (DATA) for bi-directional data communication with main memory 104. A memory controller 112 controls data communication between the memory 100 and external devices by responding to control signals (CONTROL SIGNALS).

Cache memory 102 comprises a plurality of fast static registers or channels, such as channels 102a-n. Each of the channels 102a-n is controlled by a channel controller, indicated by 103a-n. Because each of the channels 102a-n has its own controller , the channel 102a-n operates independently from each other and provide fast access paths between main memory 104 and I/O buffer 106. The independent operation and fast access path of each of the channels collectively result in a higher memory bus bandwidth and reduced data access latency of the memory device. A memory device which includes a cache memory such as that of memory device 100 is commonly referred to as virtual channel memory (VCM) device.

Figure 2 illustrates a memory device 200 of the invention. Memory device 200 comprises a memory chip 201. Memory device is similar to memory device 100 of Figure 1 with an exception of an additional feature indicated by a compression and decompression (C/D) engine 214. C/D engine 214 itself is well known to those skilled in the art. C/D engine 214 is connected between a main memory 204 and a cache

memory 202 which is connected to an I/O buffer 206. Main memory comprises one or more addressable memory banks, indicated by BANK 1-N. Each of the memory banks BANK 1-N comprises a plurality of memory cells arranged in rows and columns. Row decode circuit 208 and column decode circuit 210 access the rows and columns in response to an address, provided on address bus (ADDRESS) by an external controller, such as a microprocessor. I/O data buffers 206 connects to data communication lines (DATA) for bi-directional data communication with main memory 204. In addition, a memory controller 212 controls data communication between the memory 200 and external devices by responding to control signals (CONTROL SIGNALS).

Cache memory 202 may be selected from any type of memory but usually a static random access memory (SRAM) and normally operates at a faster speed than main memory 204, which is typical a dynamic random access memory (DRAM). Cache memory 202 may comprise one or more registers or channels as indicated in the Figures as channels 206a-n. Each of the channels is controlled by a channel controller 203a-n.

The inclusion of C/D engine 214 in a single chip, chip 201, with main memory 204 and cache memory 202 is practicable in this memory device because cache memory 204, having reduced data access latency, would hide or compensate any data access latency associated with C/D engine 214. Furthermore, the inclusion of C/D engine on the same chip with the main memory and the cache memory increases the operational speed of the memory device by eliminating off-chip drivers and connections.

As its name indicates, a C/D engine is a device which compresses and decompresses data using a hardware encoding scheme such as a Lempel Ziv encoding or other industry standard encoding schemes. One advantage of using a C/D engine, such as C/D engine 214, in a DRAM device is that data is compressed through the C/D before it enters main memory 204. This in effect increases a storage density of main memory 214.

In operation, I/O buffer 206 receives data from data communication lines DATA. Cache memory 202 processes the data and produces processed data. C/D engine 214 receives the processed data from cache memory 202 and compresses the

data before it is stored or written into main memory 204. The data stored in main memory 204 can be read and decompressed.

Figure 3 illustrates another memory device according to the invention. Memory device 300 is similar to memory 200 of Figure 2 with the exception of an error detection and correction (ECC) engine 302. ECC engine 302 is connected between C/D engine 214 and main memory 204. As in the case with the C/D engine, several types of ECC engines are well known to those skilled in the art. ECC engine 302, in memory device 300 will ensure the accuracy of data without substantially compromising a functional operation of the memory device, such as speed or latency, because cache memory 214 would reduce or compensate any latency which the ECC engine may produce. Furthermore, all the components of memory device 300 in Figure 3 are in a single chip, indicated by chip 301.

An ECC engine is a device which performs a process of detecting for error and correcting the error to ensure the accuracy and integrity data during a data transmission. Any ECC engine using Hamming Code, Reed-Solomon Code or other techniques can be used as ECC engine 302 in memory device 300 of the invention.

The inclusion of the C/D engine and the ECC engine in a memory device of the present invention as described above is not limited to memory devices having a cache memory or virtual channel memory. The C/D and the ECC engines may also be included in other memory devices including, but not limited to Double Data Rate synchronous DRAM (DDR SDRAM) or DRAM devices similar to RDRAM (TM) made by Rambus (TM) corporation.

Figure 4 illustrates a memory device of the invention having a C/D and the ECC engines included in a DRAM device other than a virtual channel memory device. Memory device 400 may be a DDR SDRAM device or an RDRAM (TM) device with the exception of C/D engine 414 and the ECC engine 402 connected between a main memory 404 and I/O buffer 406. Main memory comprises one or more addressable memory banks, indicated by BANK 1-N. Each of the memory banks BANK 1-N comprises a plurality of memory cells arranged in rows and columns. Row decode circuit 408 and column decode circuit 410 access the rows and columns in response to

an address, provided on address bus (ADDRESS) by an external controller, such as a microprocessor. I/O data buffers 406 connect to data communication lines (DATA) for bi-directional data communication with main memory 404. A memory controller 412 controls the operation of the memory via control signals, indicated as CONTROL SIGNALS. In addition, all the components of memory device 400 are in a single chip, indicated by chip 401.

Figure 5 illustrates a system 500 which includes a memory device 502 connected to an external processor 504. Memory device 502 may be one or more of any of the memory devices of the present invention described above. Memory 502 communicates with processor 504 via an address bus (ADDRESS) and a data bus (DATA) and control signals which include, but are not limited to, a Chip Select (CS*), a Clock (CLK), Row Access Strobe (RAS*), Column Access Strobe (CAS*), Write Enable (WE*), Clock Enable (CKE).

Figure 6 illustrates an embodiment of an exemplary environment of the invention. The embodiment includes a computer system 600 including one or more of the memory devices of the present invention. Computer 600 comprises a processor 602 connected to a memory device 604. Memory device 604 may be any of the memory devices of the invention described above. Memory device 604 is used for storing data or for other application within the system. Because of its high density, high bandwidth and reduced data access latency, memory device 604 can be used as random access memory of the computer system to improve the overall performance of the computer system. Memory device 604 can also improve the processing of graphic information or video information by storing more information and operating at reduced latency. Therefore memory device can be connected to a graphic control card 606 or a video control card 608 for use in processing graphic or video information.

Conclusion

Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment

shown. This application is intended to cover any adaptations or variations of the present invention. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A memory device comprising:

a main memory;

a cache memory connected to the main memory; and

a compression and decompression engine connected between the main memory and the cache memory.

2. The memory device of claim 1 further comprising an error detection and correction engine connected to the main memory and the compression and decompression engine.

3. The memory device of claim 2 wherein the main memory, the cache memory, the compression and decompression engine, and the error detection and correction engine are in the same chip.

4. A memory device comprising:

a main memory;

a cache memory connected to the main memory;

a compression and decompression engine connected between the main memory and the cache memory; and

an error detection and correction engine connected to the main memory and the compression and decompression engine.

5. The memory device of claim 4 wherein the error detection and correction engine is connected between the main memory and the compression and decompression engine.

6. A memory device comprising on a single semiconductor chip:

an input/output buffer;

a cache memory connected to the input/output buffer;

a compression and decompression engine connected to the cache memory; and

a main memory connected to the compression and decompression engine.

7. The memory device of claim 6 wherein the compression and decompression engine is connected between the main memory and the cache memory.

8. The memory device of claim 7 further comprising a error detection and correction engine connected to the main memory and the compression and decompression engine.

9. A system comprising:

a processor; and

a memory device connected to the processor, wherein the memory device comprising a main memory and a compression and decompression engine connected to the main memory.

10. The system of claim 9 wherein the memory device further comprises an error detection correction engine connected to the compression and decompression engine.

11. A system comprising:

a processor;

a cache memory; and

a memory device connected to the processor, wherein the memory device comprises a main memory, a compression and decompression engine connected to the main memory and a cache memory connected to the compression and decompression engine.

12 The system of claim 11 wherein the memory device further comprises an error detection correction engine connected to the compression and decompression engine.

13. The system of claim 11 further comprising a graphic control card, wherein the graphic control card connects to the memory device.

14. The system of claim 11 further comprising a video control card, wherein the video control card connects to the memory device.

15. A method of increasing a storage density of a memory device, comprising:
forming a main memory in a semiconductor chip;
forming a compression and decompression engine in the same chip; and
connecting the compression and decompression engine to the main memory.

16. The method of claim 15 further comprising:
forming a cache memory in the same chip; and
connecting the cache memory to the compression and decompression engine.

17. The method of claim 15 further comprising:
providing an error detection and correction engine; and
connecting the error detection and correction engine to the compression and decompression engine.

18. A method of operating a memory device, comprising:
receiving input data at a cache memory;
compressing the data at a compression and decompression engine to produce compressed data; and
storing the compressed data into a main memory;

19. The method of claim 18 further comprising:
reading the compressed data from the main memory;
decompressing the data at the compression and decompression engine to produced decompressed data; and

reading the decompressed data to the cache memory.

20. A method of operating a memory device, comprising:

forming an input/output buffer;

receiving data at the input/output buffer;

processing the data at a cache memory to produce processed data;

compressing the processed data at a compression and decompression engine to produce compressed data; and

storing the compressed data into a main memory.

21. The method of claim 20 further comprising:

reading data from memory;

decompressing the data at the compression and decompression engine to produced decompressed data;

reading the decompressed data at the cache memory; and

transferring the data to the input/output buffer.

Abstract of the Disclosure

A memory device comprising a compression and decompression engine and a error detection and correction engine connected between a cache memory and a main memory in the same semiconductor chip.

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Date of Deposit: March 3, 2000

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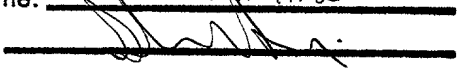
Printed Name: Shalyn Hise

Signature: 

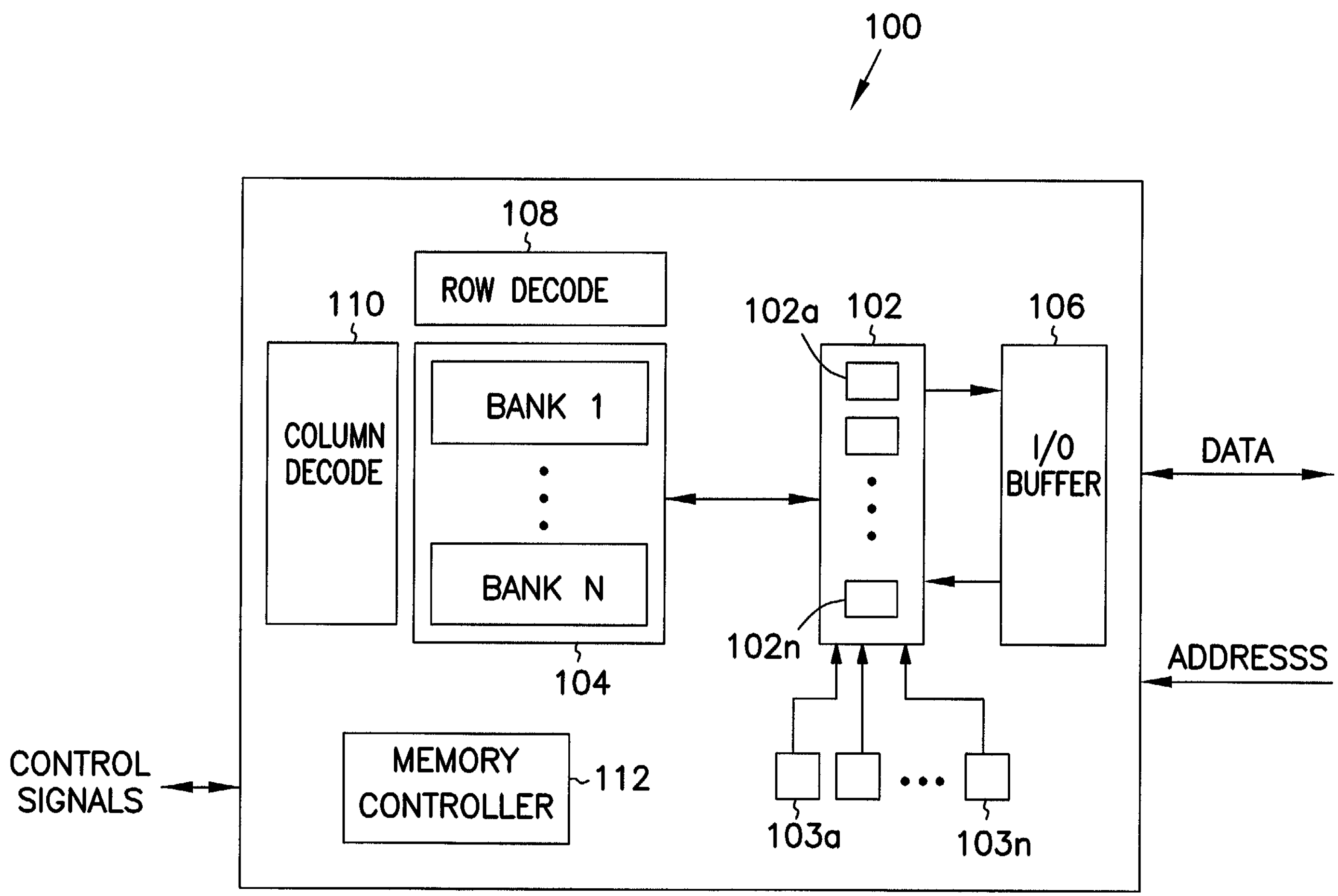
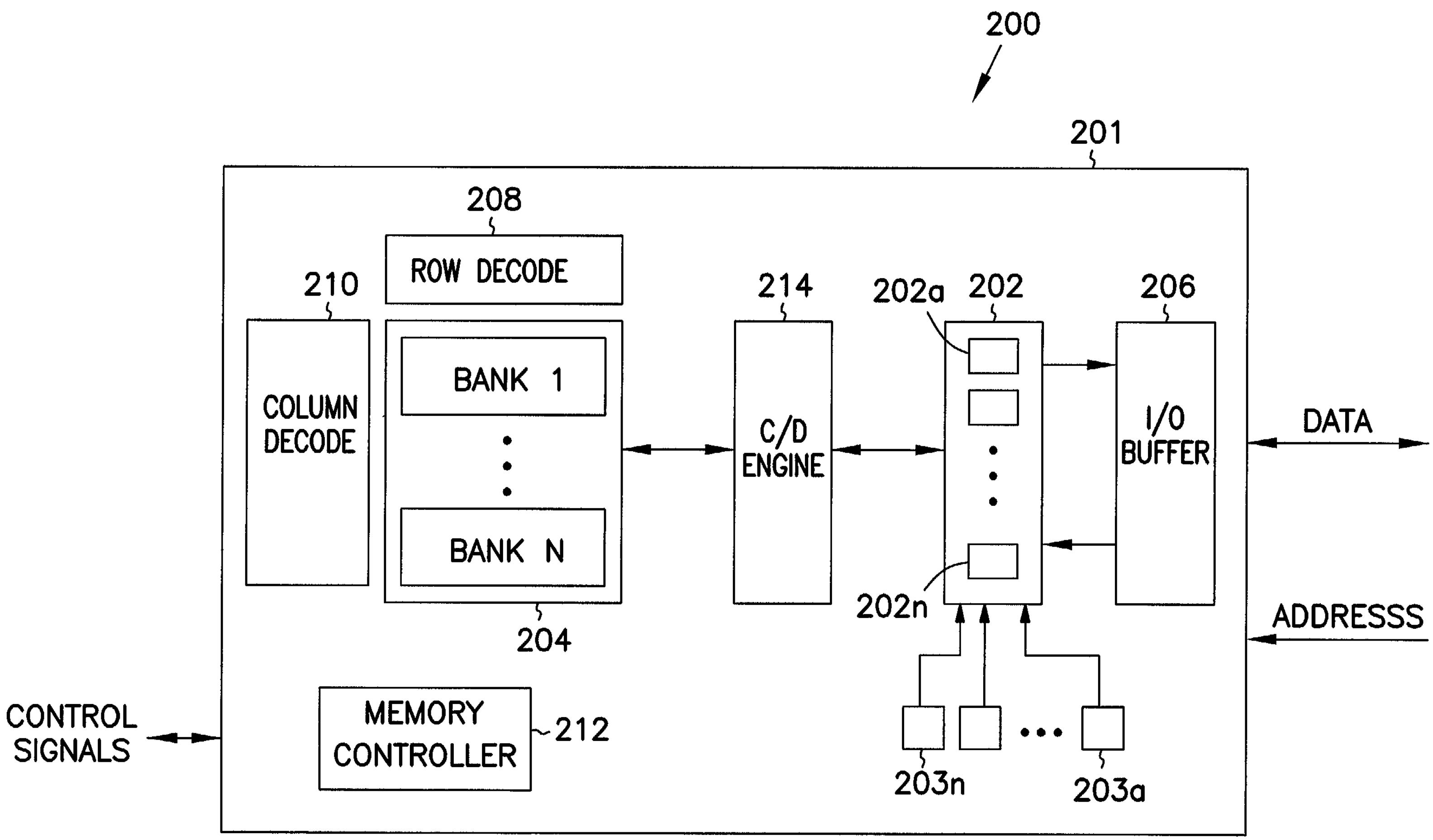


FIG. 1
(Prior Art)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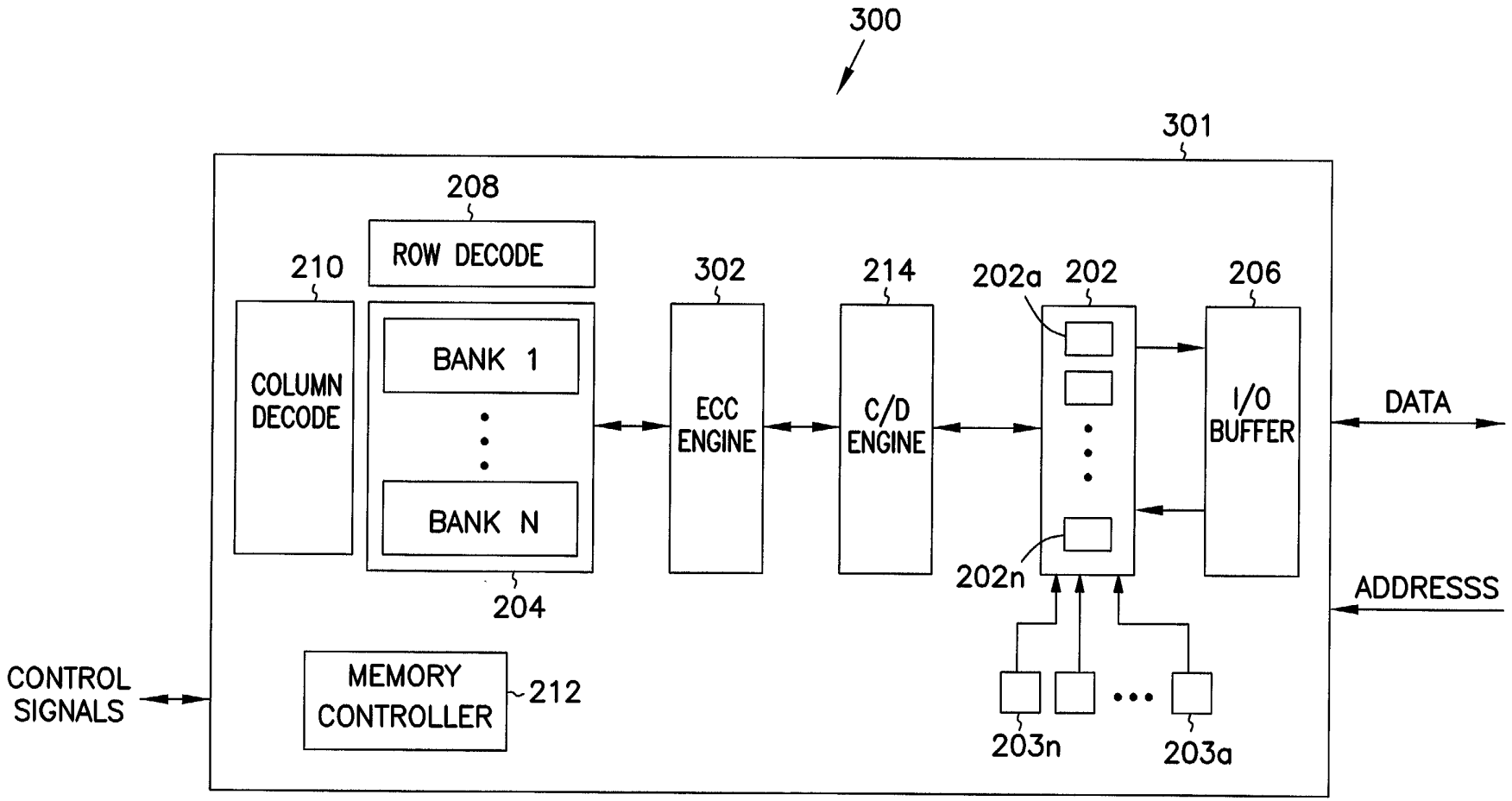
201
208
ROW DECODE
210
COLUMN DECODE
BANK 1
BANK N
204
214
C/D ENGINE
202a
202
202n
206
I/O BUFFER
DATA
ADDRESSS
CONTROL SIGNALS
MEMORY CONTROLLER
212
203n
203a

FIG. 2


300
301
208
ROW DECODE
210
COLUMN DECODE
BANK 1
BANK N
204
302
ECC ENGINE
214
C/D ENGINE
202a
202
202n
206
I/O BUFFER
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CONTROL SIGNALS
MEMORY CONTROLLER
212
203n
203a

FIG. 3

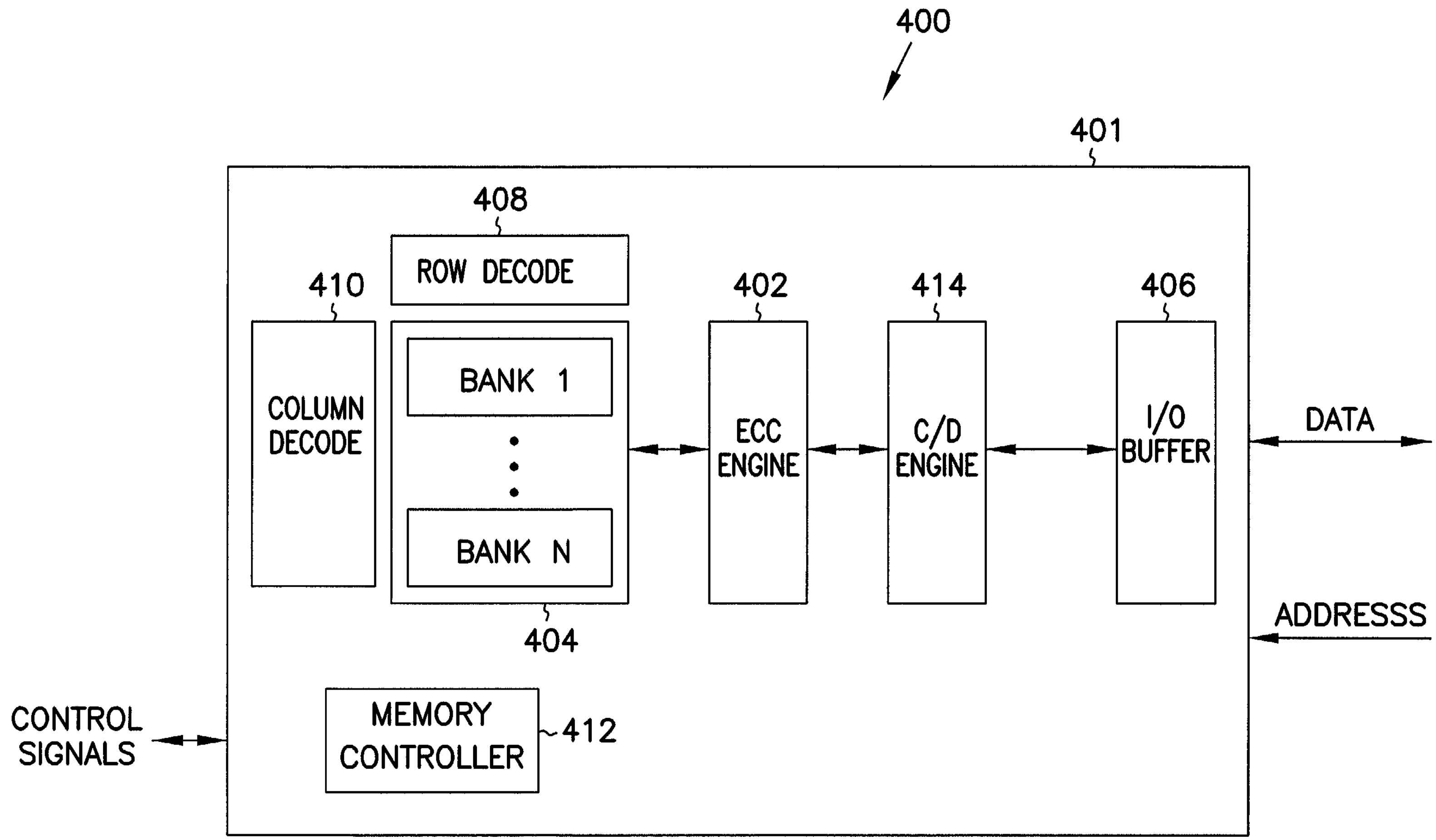
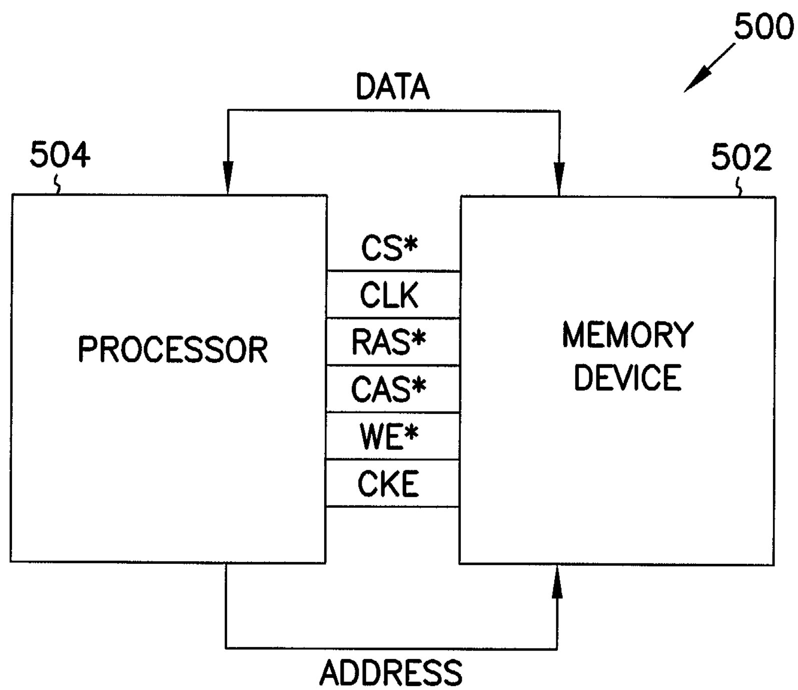

400
401
408
ROW DECODE
410
COLUMN DECODE
BANK 1
BANK N
404
402
ECC ENGINE
414
C/D ENGINE
406
I/O BUFFER
DATA
ADDRESSS
CONTROL SIGNALS
MEMORY CONTROLLER
412

FIG. 4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DATA
504
502
PROCESSOR
CS*
CLK
RAS*
CAS*
WE*
CKE
MEMORY
DEVICE
ADDRESS

FIG. 5

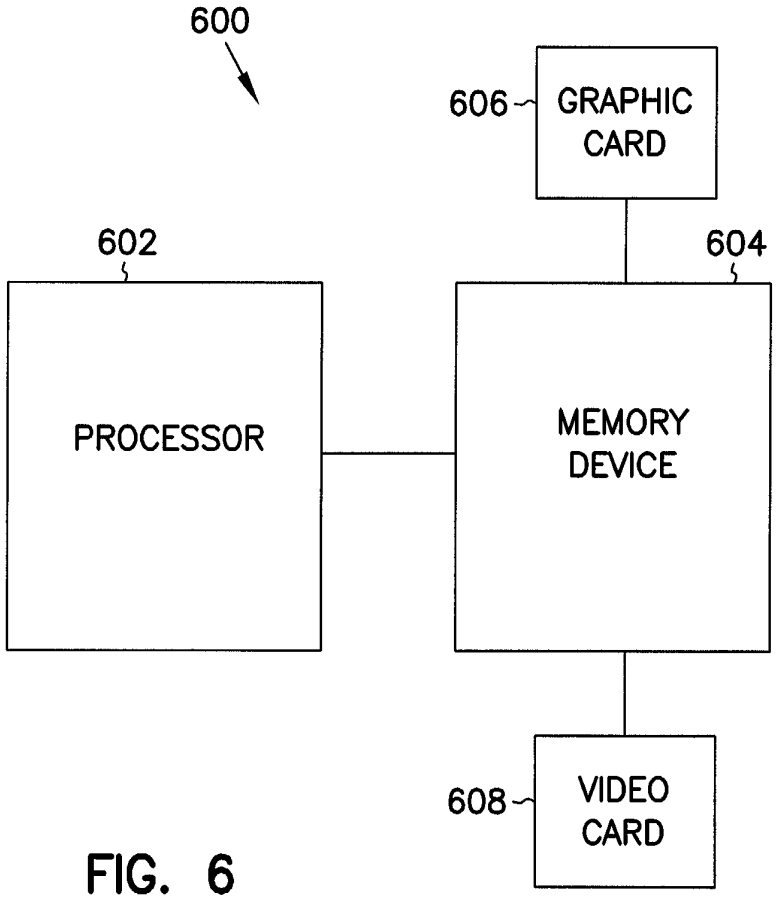
600
606
GRAPHIC CARD
602
604
PROCESSOR
MEMORY DEVICE
608
VIDEO CARD

FIG. 6

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH DENSITY STORAGE SCHEME FOR SEMICONDUCTOR MEMORY .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Eugene H. Cloud**
Citizenship: **United States of America** Residence: **Boise, ID**
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Boise, ID 83712

Signature: Eugene H Cloud Date: 3-1-00
Eugene H. Cloud

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.